Amendments to the Specification:

IN THE SPECIFICATION

Please replace original paragraph **[0026]** with the following currently amended paragraph **[0026]** provided below:

[0026] Memory circuit 100 includes sense circuit 112. Sense circuit 112 is coupled to array 102 and outputs data during a read operation. Sense circuit 112 is coupled to output port 114 as signal DATA OUT. In one embodiment, sense circuit 112 is constructed according one of the embodiments shown and described in co-pending Application Serial No. 10/614,581, filed on ~~even date herewith~~ July 7, 2003, entitled: Memory Cell Strings In A Resistive Cross Point Memory Cell Array, attorney docket no. 200208506-1 (the '506 Application). The '506 Application is incorporated herein by reference.

Please replace original paragraph **[0040]** with the following currently amended paragraph **[0040]** provided below:

[0040] Figure 5 is a block diagram of a sense circuit, indicated generally at 500, for use with an array of complementary memory cells according to one embodiment of the present invention. Sense circuit 500 includes input 501 that is adapted to receive an input from an array of memory cells, e.g., from sense point $V_{SE\,NSE}$ of a sense line of array 200 of Figure 2. Sense circuit 500 includes sample and hold circuit 502 and comparator 504. Input 501 is provided to both sample and hold circuit 502 and comparator 504. Further, sample and hold circuit 502 is coupled to another input of comparator 504. Comparator 504 provides an output 505 for sense circuit 500.